WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

partially reconfigurable programmable circuit elements; and

a finite state machine,

wherein the finite state machine configures the partially reconfigurable programmable circuit elements to detect boundaries between words in an input data stream,

the finite state machine determines when the partially reconfigurable programmable circuit elements correctly indicate boundaries between frames in the input data stream, and

the finite state machine reconfigures the partially reconfigurable programmable circuit elements to align the words in the input data stream based on the detected word boundaries and to determine when the word boundaries have changed.

2. The integrated circuit according to claim 1 further comprising:

data and overhead processing circuitry.

3. The integrated circuit according to claim 1 further comprising:

input/output circuitry that receives the input data stream.

4. The integrated circuit according to claim 1 wherein the integrated circuit includes portions of hardwired, application-specific circuitry.

5. The integrated circuit according to claim 1 wherein the integrated circuit is a field programmable gate array.

6. The integrated circuit according to claim 1 wherein:

the finite state machine reconfigures the partially reconfigurable programmable circuit elements to locate framing patterns in SONET input data.

7. The integrated circuit according to claim 6 wherein:

the finite state machine reconfigures the partially reconfigurable programmable circuit elements to align frames in the SONET input data stream based on the detected boundaries.

8. The integrated circuit according to claim 1 wherein:

the finite state machine reconfigures the partially reconfigurable programmable circuit elements to locate framing patterns in SDH frames in the input data stream.

9. The integrated circuit according to claim 8 wherein:

the finite state machine reconfigures the partially reconfigurable programmable circuit elements to align frames in the SDH input data based on the detected boundaries.

10. The integrated circuit according to claim 1 wherein:

the finite state machine reconfigures the partially reconfigurable programmable circuit elements to locate training patterns in OIF SPI4 phase 2 input data.

11. The integrated circuit according to claim 10 wherein:

the finite state machine reconfigures the partially reconfigurable programmable circuit elements to align channels in the OIF SPI4 phase 2 input data based on the detected training patterns.

12. A method comprising:

configuring reconfigurable programmable circuit elements to detect boundaries between words in input data using a finite state machine, wherein the finite state machine determines when the reconfigurable programmable circuit elements correctly indicate boundaries between frames in the input data; and

reconfiguring the reconfigurable programmable circuit elements to align the words in the input data based on the detected word boundaries and to determine when the word boundaries have changed using the finite state machine.

13. The method of claim 12 further comprising:

processing overhead and data bytes in the input data using data and overhead processing circuitry.

14. The method of claim 12 further comprising:

receiving the input data at input/output circuitry.

15. The method of claim 12 wherein the integrated circuit includes portions of hardwired, application-specific circuitry.

16. The method of claim 12 wherein the integrated circuit is a field programmable gate array, and the reconfigurable programmable circuit elements are partially reconfigurable.

17. The method of claim 12 wherein reconfiguring the partially reconfigurable programmable circuit elements further comprises:

reconfiguring the partially reconfigurable programmable circuit elements to locate framing patterns in SONET input data using the finite state machine.

18. The method of claim 17 wherein reconfiguring the partially reconfigurable programmable circuit elements further comprises:

reconfiguring the partially reconfigurable programmable circuit elements to align frames in the SONET input data stream based on the detected boundaries.

19. The method of claim 12 wherein reconfiguring the partially reconfigurable programmable circuit elements further comprises:

reconfiguring the partially reconfigurable programmable circuit elements to locate framing patterns in SDH input data using the finite state machine.

20. The method of claim 19 wherein reconfiguring the partially reconfigurable programmable circuit elements further comprises:

reconfiguring the partially reconfigurable programmable circuit elements to align frames in the SDH input data based on the detected boundaries.

21. The method of claim 12 wherein reconfiguring the partially reconfigurable programmable circuit elements further comprises:

reconfiguring the partially reconfigurable programmable circuit elements to locate training patterns in OIF SPI4 phase 2 input data.

22. The method of claim 20 wherein reconfiguring the partially reconfigurable programmable circuit elements further comprises:

reconfiguring the partially reconfigurable programmable circuit elements to align channels in the OIF SPI4 phase 2 input data based on the detected training patterns.